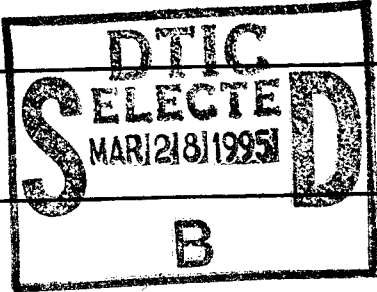


REPORT DOCUMENTATION PAGE			Form Approved OMB No. 0704-0188	
<small>Public reporting burden for this collection of information is estimated to average 1 hour per response, including the time for reviewing instructions, searching existing data sources, gathering and maintaining the data needed, and completing and reviewing the collection of information. Send comments regarding this burden estimate or any other aspect of this collection of information, including suggestions for reducing this burden, to Washington Headquarters Services, Directorate for Information Operations and Reports, 1215 Jefferson Davis Highway, Suite 1204, Arlington, VA 22202-4302, and to the Office of Management and Budget, Paperwork Reduction Project (0704-0188), Washington, DC 20503.</small>				
1. AGENCY USE ONLY (Leave blank)	2. REPORT DATE 11/18/94	3. REPORT TYPE AND DATES COVERED Final - 7/1/93 - 6/30/94		
4. TITLE AND SUBTITLE Studies of Lattice-Mismatched and Low-Temperature-Grown Semiconductor Multiple-Phase Systems		5. FUNDING NUMBERS AFOSR-91-0327 61102P 2305/BS		
6. AUTHOR(S) Professor J.S. Smith Professor E. Weber		8. PERFORMING ORGANIZATION REPORT NUMBER 442427-22518 AFOSR-TR- 95 0124		
7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES) The Regents of the University of California c/o Sponsored Projects Office 336 Sproul Hall Berkeley, CA 94720		10. SPONSORING/MONITORING AGENCY REPORT NUMBER AFOSR 91-0327 61102P		
9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES) AFOSR Bolling AFB, DC 20322-6448		11. SUPPLEMENTARY NOTES n/a		
12a. DISTRIBUTION/AVAILABILITY STATEMENT Approved for Public Release Distribution unlimited				
12b. DISTRIBUTION CODE		13. ABSTRACT (Maximum 200 words) The research efforts for this project were aimed at implementing novel concepts in the integration of GaAs and Si structures for optoelectronic applications. A major breakthrough in the area of nanofabrication of foreign microstructures on host substrates was achieved.		
14. SUBJECT TERMS GaAs/Si structures for optoelectronic applications, fluidic integration, self-assembly, monolithic		15. NUMBER OF PAGES 13		
17. SECURITY CLASSIFICATION OF REPORT		16. PRICE CODE		
18. SECURITY CLASSIFICATION OF THIS PAGE		20. LIMITATION OF ABSTRACT		
19. SECURITY CLASSIFICATION OF ABSTRACT				

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INTRODUCTION

AFOSR-TR- 95 01 14

In the final year of this contract, the research efforts for this project were aimed at implementing novel concepts in the integration of GaAs and Si structures for optoelectronic applications.

We have achieved a major breakthrough in the area of nanofabrication of foreign microstructures on host substrates. We are applying for broad patent rights on the technique, and it appears to have many applications, III-V devices on silicon as well as other applications such as active matrix LCD displays. We successfully demonstrated the technique in the lab for LEDs and tunneling diodes, long wavelength detectors, and tunneling diodes. This method has broad implications for integration of many material systems and growth techniques.

I. Fluidic Self Assembly

Fluidic self assembly is a vastly improved method for manufacture of microscopic assemblies, including integration of electronic, mechanical, and optical devices on silicon, or of silicon electronic chips onto plastic or other substrates such as active matrix LCDs.

The process works automatically, using random fluidic transport, allowing the placement of large numbers of devices in minutes. Fluidic self assembly takes advantage of hydrodynamic steering to place a slurry of microscopic blocks, each with a completed device or circuit, filling an array of sites on a target substrate. Micromachining techniques are used to form the trapezoidal blocks from almost any epitaxial technology, and the sites on the target substrate have been formed using selective etching on silicon, and can probably

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be easily formed by molding or stamping in plastic substrates. The equipment used for the fluidic assembly process itself is simple, consisting of bubble pumps, reservoirs, and substrate holders. The process is intrinsically stochastic, rather than deterministic, but high yields (99%) of correctly assembled devices have been demonstrated for blocks ranging in size from 20 microns to 1 millimeter on a side, a range of 10^5 in mass. Higher yields are theoretically possible, and bonding and additional fluidic passes could fill empty sites. High single assembly yields have been demonstrated for two fold as well as four fold rotation symmetry. Two fold rotation symmetry placement is accomplished with rectangular blocks and sites. Tested aspect ratios range from 1:2 and 1:4.5, top size to thickness. Positioning accuracy only depends on the lithographic and micromachining accuracy for the sites and blocks, which can be accurate to within a micron.

The cost reduction comes from the great efficiency of the use of the wafer area of the emplaced devices. The devices are fabricated at extremely high packing densities, and then inexpensively placed only where desired on the target substrate.

This should allow manufacture active of matrix large liquid crystal displays at significantly reduced cost. Single crystal silicon circuits (smart pixels) would be placed as desired onto stamped plastic substrates.

Fluidic self assembly could also be applied to new pixel technologies such as LED elements, or even mixed elements by fluidically assembling the display elements themselves. This would allow, for example, separate grow of red, green, and blue LEDs, along with silicon electronics, grown and fabricated on native substrates and assembled into a complete display.

II. InGaAs/GaAs Heteroepitaxy

The ability to grow high In-content $\text{In}_x\text{Ga}_{1-x}\text{As}$ is highly desirable for lasers, modulators, or detectors operating at $1.3\ \mu\text{m}$ or $1.55\ \mu\text{m}$. Currently, this is achieved using the InP material system. This system, however, is more expensive and less mechanically robust than the GaAs system. If this material can be grown on GaAs, then GaAs devices can also be integrated. The main drawback to this approach is the large lattice mismatch between $\text{In}_x\text{Ga}_{1-x}\text{As}$ ($x > 0.05$) and GaAs. Depending on the desired Indium content, the critical thickness can be as small as a few monolayers.

Out of all the methods tried so far, the linearly graded buffer offers the most promise. Whereas a step grade bends threading dislocations away, a linear grade improves upon this by also preventing dislocation loops from forming and by causing already-present dislocations to glide out to the edge instead of up to the surface (J. Tersoff, *Appl. Phys. Lett.* **62** 693 (1993)). Lord *et al.* (*Electron. Lett.* **28** 1193 (1992)) demonstrated the viability of this technique by fabricating detectors on $\text{In}_x\text{Ga}_{1-x}\text{As}$ that was linearly graded to $x=0.4$. These detectors operated with quantum efficiencies of 27% at $1.2\ \mu\text{m}$, and 9% at $1.3\ \mu\text{m}$. Nevertheless, the surface was still highly cross-hatched which indicates that a large number of dislocations were still propagating to the surface.

To improve the morphology and the crystal quality, we have introduced strained-layer superlattices (SLS) into the linearly graded buffer. Whereas the linear grade will result in cross-hatching, the inclusion of SLS will give a shiny surface. Under Nomarski, slight cross-hatching becomes visible, but the morphology still looks better than the sample with the simple linear grade. From this reduction in cross-hatching, it is seen that the superlattices

appear to be bending the dislocations away. More work needs to be done to better investigate the effects of the superlattices.

To test the device quality of this material, we fabricated *p-i-n* photodetectors with an x content of 0.4. Comparing samples with and without the SLS, we found that devices with the SLS had an order of magnitude reduction in the dark current (from $31.7 \mu\text{A}$ down to $1.897 \mu\text{A}$ at a bias voltage of -3 V). Similarly, the breakdown performance improved dramatically for the sample with the SLS. In this case, V_{bd} increased from -5 V to over -15 V . Because of this, the devices without the SLS were too noisy to accurately test for their quantum efficiencies. The spectral response of all the detectors showed a peak sensitivity around $1.1\text{--}1.3 \mu\text{m}$, with abrupt cutoffs at wavelengths corresponding to below-bandgap energies. For the devices with the SLS, we measured the quantum efficiency η to be 32.3% at $1.2 \mu\text{m}$ with $V_b = -10 \text{ V}$, and 16.9% at $1.3 \mu\text{m}$ with $V_b = -14 \text{ V}$. In doing these measurements, the 30% reflection at the air-device interface was taken into account. Again, we see that the presence of the SLS resulted in a marked improvement in the device performance.

III. Fluidic Self-Assembly of GaAs and InGaAs Photodetectors onto a Si Substrate

We have investigated the integration of III-V devices onto Si using fluidic self-assembly (FSA). To demonstrate the feasibility of this technique, we have integrated photodetectors made from both GaAs and InGaAs onto a Si substrate. First, devices were grown on GaAs using MBE. The structure grown consisted of a 1.5 μm -thick AlAs lift-off layer followed by the actual photodetector. Since the InGaAs detector was designed to operate at 1.3 μm , a linearly graded buffer with strained-layer superlattices was used to grade from $x=0$ to $x=0.4$. The total thickness of all the detectors was chosen to be 10 μm . After growth, the surface was metallized with Au, and then standard photolithography was used to form mesas. The dimensions after etching were 10 $\mu\text{m} \times 10 \mu\text{m}$ at the mesa tops and 20 $\mu\text{m} \times 20 \mu\text{m}$ at the mesa bottom. These wafers were then glued face down onto a dummy Si wafer with commercially available Tech Wax. The wafers were lapped and selectively etched to reveal the AlAs lift-off layer which was subsequently removed by etching in HF. A second lithography was used to form ring contacts on the now-exposed backside. The blocks were freed from the wax and placed in a carrier liquid (in this case, ethanol). This liquid was decanted over a Si wafer with 10 μm deep holes etched into it to allow the blocks to fall in the holes.

The yields are still low since we are just using one pass to fill as many of the holes as possible. Using a recirculation scheme where unused blocks can be collected and passed over the surface again, the yields should go up. The detectors that did self-assemble demonstrated typical diode I-V characteristics. Both the GaAs and InGaAs photodetectors demonstrated photoresponse when illuminated with white light (on the order of 100 nA at a reverse bias of -3 V). Due to the size of the devices, we were not able to test the spectral response or

calculate the quantum efficiency. We are currently working on a planarization and bonding scheme that will allow us to make measurements without using a probe station. Also, to facilitate the testing, we are also working on $40\text{ }\mu\text{m}\times 40\text{ }\mu\text{m}$ devices.

IV. Growth of Strain-Free GaAs on Si/Sapphire

GaAs on Si heteroepitaxy has suffered from the high density of threading dislocations and the large residual tensile strain in GaAs films on Si substrates. The problem of high residual strain in GaAs films, attributed to the differential thermal contraction between GaAs and Si during cooling-down after growth, needs to be solved in order to realize high quality minority carrier devices in addition to reduction of dislocation densities. For reducing the high residual strain, post-growth patterning, growth on patterned substrates, and strain compensation have been employed in our previous research. For reducing thermal strain, sapphire is an attractive substrate because its thermal expansion coefficient ($\simeq 7.5 \times 10^{-6} / ^\circ\text{C}$) is comparable to that of GaAs ($\simeq 6.3 \times 10^{-6} / ^\circ\text{C}$). GaAs epitaxial films were grown on [001]-Si/[1 $\bar{1}$ 02]-Sapphire substrates (SOS), using MBE. In order to increase the heating efficiency of the substrates, (100 nm Ti/3 μm Si) films were deposited on the back of sapphire. With these layers, we could grow GaAs on SOS using the same two-step growth conditions we normally use for GaAs on Si.

From 77K photoluminescence(PL), GaAs films grown on SOS show compressive residual strain (which contradicts the findings of other groups but is expected from the thermal contraction calculations), while GaAs films grown on Si show tensile strain. The magnitude of the compressive residual strain in GaAs grown on SOS was estimated to be 5×10^{-4} and was about one order smaller than that in GaAs/Si. The intensity of the PL peak of GaAs/Si/Sapphire at 77K was comparable or stronger than peaks from GaAs/Si. Full Width at Half Maximum (FWHM) of 77K PL was about 15 meV in GaAs/SOS and 8 meV

in GaAs/GaAs. These imply that the quality of GaAs on SOS was better than GaAs grown on Si substrates but still highly defective compared to GaAs/GaAs films.

Residual strain in GaAs films on Si/Sapphire could be reduced further by applying the strain compensation method, which we reported in the previous reports. The strain in GaAs on SOS was compressive in nature. Hence, misfit strain, that has the same magnitude as the thermal strain but is opposite in sign, can compensate the thermal strain. InGaAs films were used as buffer layers to induce tensile misfit strain in GaAs grown on SOS.

77K PL was used to compare the strain in GaAs layers grown on SOS with InGaAs buffer layers of different Indium contents. As the Indium content was increased above 1%, the strain in GaAs on SOS was changed from compressive to tensile. When an InGaAs layer with 0.6% Indium was grown as a buffer layer, GaAs films on InGaAs/Si/Sapphire showed the same peak position as that of GaAs/GaAs which implied that GaAs films on InGaAs/Si/Sapphire were strain-free.

The maximum thickness of strain-free GaAs is determined by monitoring PL peak positions versus the thickness of GaAs films grown on $\text{In}_{0.006}\text{Ga}_{0.994}\text{As/Si/Sapphire}$. There was no change in PL peak positions from GaAs films with thicknesses up to $0.4\text{ }\mu\text{m}$, which indicates that the strain-free state was maintained up to that thickness.

During the growth of GaAs on Si/Sapphire, we could observe 4×4 surface reconstruction from Reflection High Energy Electron Diffraction (RHEED), which can be considered as an overlap of 2×4 and 4×2 diffraction patterns. Also, surface morphology showed regular patterns on the GaAs surfaces which are parallel to $\langle 110 \rangle$ directions. From chemical etching,

we could observe a high density of antiphase domains, which may be due to the fact that the surface orientation of Si was close to (001).

In summary, GaAs epitaxial films grown on Si/Sapphire wafers using MBE showed compressive residual strain with a magnitude about one order smaller than that in GaAs/Si. By using InGaAs layers as buffer layers, the compressive thermal strain in GaAs grown on InGaAs/SOS could be compensated by misfit strain to produce a 0.4 μm thick strain-free GaAs film on Si/Sapphire.

V. Electrical and Structural Properties of Low Temperature (LT) $\text{Al}_x\text{Ga}_{1-x}\text{As}$

Low temperature (LT) MBE-grown GaAs has attracted much attention in recent years, due to its unique material and device attributes. Specifically, the semi-insulating property of LT GaAs in its annealed state has been extensively characterized. Although the exact origin of this property is still an open question, it is generally accepted that this effect is in some way related to the incorporation of excess arsenic in the material during growth. This excess As has also been held responsible for the lattice dilation which is observed in as-grown LT GaAs layers.

LT $\text{Al}_x\text{Ga}_{1-x}\text{As}$ layers are known to exhibit properties similar to those of LT GaAs. However, very little detailed study has been made of the similarities and differences between these two materials. One focus of our research has thus been the electrical and structural characterization of LT $\text{Al}_x\text{Ga}_{1-x}\text{As}$, using experimental techniques such as current-voltage, temperature-dependent conductivity, and high-resolution x-ray diffraction measurements, in conjunction with computer-aided modeling of the materials.

Through I-V measurements made on simple n-i-n resistor structures, we have shown that annealed LT $\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}$ exhibits extremely large low-field resistivity, on the order of 10^{11} to $10^{12} \Omega \text{ cm}$. We attribute this high value to a very large deep donor activation energy of approximately 1.0 eV in LT $\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}$, as determined from temperature-dependent conductivity measurements. In addition, experimental I-V and σ -T characteristics for these LT $\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}$ layers are shown to exhibit evidence of hopping behavior at room temperature. A simple computer-aided analysis of these data yields a deep trap concentration N_T of approximately 10^{18} cm^{-3} , and a compensating acceptor concentration N_A of approximately

10^{16} eV. The occurrence of hopping at room temperature is attributed to the high activation energy of the traps, which results in a reduction of electron conduction through the conduction band. The contribution of hopping to the measured conductivity thus becomes significant at higher temperatures.

Using high resolution x-ray diffraction techniques, we have also studied the lattice parameter behavior of low-temperature $\text{Al}_x\text{Ga}_{1-x}\text{As}$ as a function of temperature and aluminum content. Similar to LT GaAs, the as-grown LT $\text{Al}_x\text{Ga}_{1-x}\text{As}$ layers exhibit a dilated lattice constant which, upon annealing, contracts to that of “normal” material. The onset of this contraction in LT $\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}$, however, is found to occur at an annealing temperature nearly 100°C higher than that required for LT GaAs. In addition, the relative lattice expansion in the as-grown LT layer is found to be a decreasing function of Al content, ranging from 0.099% for LT GaAs to 0.059% for LT $\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}$. This is attributed to lower than expected As incorporation in the LT $\text{Al}_x\text{Ga}_{1-x}\text{As}$ during growth.

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Patent:

"Fluidic Self Assembly". patent applied for 1993.